12b 100MS/s 1.1V 0.43mm² ADC optimized in a 45nm CMOS technology

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Abstract

This paper proposes a 12b 100MS/s four-step pipeline ADC optimized in a 45nm CMOS for low-power communication systems. The input SHA employs a gate-bootstrapping switch to sample wide band input signals with an accuracy of 12 bits or more. The SHA and MDACs adopt a two-stage amplifier with gain-boosting circuits to achieve the required DC gain and high signal swing range. Cascode and Miller frequency-compensation schemes are selectively used for wide bandwidth and stable signal settling. The constant gate and drain voltages of cascode current mirror transistors based on on-chip reference currents minimize current mismatch by process and supply variations. The prototype ADC shows a measured DNL and INL within 0.88LSB and 1.46LSB, while consuming 29.8mW at 1.1V and 100MS/s with a maximum SNDR and SFDR of 61.0dB and 74.9dB, respectively.

Keywords: Gain-boosting amplifier, Pipeline ADC.

1. Introduction

As CMOS technologies develop rapidly into nanometer-scale, analog circuits based on amplifiers suffer from a low output impedance of transistors and a reduced signal swing range from the scaled supply voltage. Thereby, it is not easy to design a high-gain, high-swing, and wide bandwidth amplifier of a high-resolution A/D converter (ADC) for communication systems. Recently, a pipeline ADC based on a range-scaling scheme has been proposed to achieve a high signal-to-noise ratio (SNR) at a low supply voltage. This scheme requires additional circuits to calibrate several reference voltages, and increases a chip area due to the number of the required capacitors [1, 2]. On the other hand, a multi-stage amplifier has been employed for a high DC gain [3]. This method needs a complicated frequency compensation technique and has the disadvantage of an increased power dissipation and lower stability. This work proposes a 45nm CMOS pipeline ADC with the amplifier design to overcome various limitations of nanometer-scale CMOS technologies at a scaled low-power supply.

2. Proposed ADC Architecture

The proposed 12b 100MS/s ADC with a four-step pipeline topology, as shown in Fig. 1, consists of an input sample-and-hold amplifier (SHA), multiplying D/A converters (MDACs), flash ADCs, a digital correction logic block with decimator, a clock generator, and on-chip current and voltage (I/V) references. The process-insensitive I/V references are implemented on chip with optional off-chip reference voltages for various system applications.

Fig. 1. Proposed 12b 100MS/s ADC based on a 45nm CMOS process.

3. Circuit Implementation

Since the input SHA and MDAC1 are the critical functional circuits that limit the performance at the pipelined ADC, the error components of the SHA and MDAC1, such as signal settling error and device non-linearity, need be minimized to improve the performance of the overall ADC.
The input SHA and MDACs of the proposed ADC essentially require a high-gain amplifier that has a wide bandwidth and a high phase margin to reduce signal settling error and to maintain a 12b linearity with low distortion. Especially, as for this MDAC1, a high DC gain of about 84dB is needed to achieve a resolution higher than 12 bits while the MDAC1 handles an input signal of 1.0Vpp at a supply voltage of 1.1V. The proposed ADC employs a two-stage amplifier with gain-boosting circuits to meet the high DC gain, wide bandwidth, and sufficient signal range regardless of process, temperature, and supply variations, as shown in Fig. 2. The first-stage amplifier is based on a folded-cascode topology with gain-boosting circuits to achieve a high DC gain of 90dB, while the second-stage amplifier employs with a differential common-source topology to meet a wide signal swing range of 1.0Vpp at a low supply voltage of 1.1V.

When using a two-stage amplifier for a high DC gain, an appropriate frequency compensation is required for stable setting behavior. Of many frequency compensation techniques for a two-stage amplifier, cascode and Miller compensation techniques have been commonly used. The cascode compensation shows a higher phase margin than the Miller compensation with the same current. However, the zero occurring from the cascode compensation is located in a lower frequency than the Miller compensation. Therefore, the SHA, requiring wide bandwidth, employs the Miller compensation with a zero-nulling resistor for stable operation. In contrast, the MDACs consuming as high power as a reduced feedback gain employ the cascode compensation [4].

Device mismatches are getting worse in nanometer-scale CMOS technologies. The variation of an output impedance due to the short channel-length modulation effect leads to a mismatch of current sources, which is one of the major factors of amplifier performance degradation. Thus, MOS transistors for the amplifier need to be composed of multiple unit devices for high matching and tracking accuracy. As a result, offset and current mismatches due to device imperfection can be minimized. The constantly maintained gate and drain voltages of transistors, M1 to M4, of the cascode current mirror in Fig. 3 reduce further the channel-length modulation and current mismatch despite process and supply variations.

4. Prototype ADC Measurements

The prototype ADC fabricated in a 45nm CMOS occupies an active die area of 0.43mm$^2$ and dissipates 29.8mW at 1.1V and 100MS/s. The measured differential and integral non-linearity (DNL and INL) is within 0.88LSB and 1.46LSB, respectively, as shown in Fig. 4. The maximum signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are measured to be 61.0dB and 74.9dB, respectively, at 100MS/s with an input frequency of 4MHz, as shown in Fig. 5. As input frequencies increase up to 50MHz at 100MS/s, the measured SNDR and SFDR with a differential input are maintained over 56.7dB and 70.2dB, as shown in Fig. 6. The measured performance of the prototype ADC is summarised in Table 1. The up-to-date reported CMOS ADCs with a 12b to 13b resolution and a sampling rate exceeding 100MS/s are compared with the proposed ADC in Fig. 7. The figure of merits (FoM), defined as Equation (1), is 0.33pJ/conversion-step, including on-chip reference circuits. The dynamic performance of the proposed ADC operating at a single supply of 1.1V is measured to be 61.0dB, which is the best value of the ADCs implemented without calibration circuit so far in a 45nm CMOS process.

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \times F_S}$$

(1)
5. Conclusion

This work describes an amplifier-based 12b 100MS/s ADC optimized in a 45nm CMOS for portable communication systems. The SHA and MDACs employ a two-stage amplifier with gain-boosting circuits for a high DC gain and wide signal swing range. Cascade and Miller frequency compensation techniques are selectively used for wide bandwidth and stable signal settling. The cascode current mirror with on-chip current references and constantly maintained gate and drain voltages of transistors reduces current mismatch due to process and supply variations. The ADC with an active die area of 0.43mm\(^2\) shows a maximum SNDR and SFDR of 61.0dB and 74.9dB, respectively, and a power consumption of 29.8mW at 1.1V and 100MS/s.

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References


